CLAIMS

What is claimed is:

1. A method for frame synchronization of a receiver in a wireless communication system wherein data is transmitted in frame units in a multipath environment, the method comprising the steps of:

extracting data samples for a predetermined window size;

generating a training sequence corresponding to a given cell parameter;

correlating the data with the training sequence over different lags to locate the position of the first significant path, which defines the beginning of the frame;

accumulating the correlated data N times, each time at a frame offset apart from the previous time, to produce at least one accumulation vector;

determining a most significant path value that is the largest value among the accumulation vectors, along with the position of the most significant path;

calculating a frame synchronization correction value based on the difference between the first significant path position and the frame offset; and

adjusting the frame synchronization based upon the frame synchronization correction value.

2. The method according to claim 1, further comprising the steps of:

separating the extracted data samples at twice the chip rate into even samples and odd samples; and

correlating the even samples separately from the odd samples.

3. The method according to claim 1, wherein the determining step includes:

calculating a preliminary noise estimate equal to the average of accumulated data values;

calculating a preliminary noise threshold equal to a multiple of the preliminary noise estimate;

calculating a final noise estimate equal to the average of accumulated data values below the preliminary noise threshold;

calculating a final noise threshold equal to a multiple of the final noise estimate; and

determining the validity of the most significant path if the most significant path value is greater than the final noise threshold.

4. The method according to claim 1, wherein the adjusting step includes delaying the frame synchronization if the frame synchronization correction value is positive.

5. The method according to claim 1, wherein the adjusting step includes advancing the frame timing if the frame synchronization correction value is negative.

6. A wireless transmit/receive unit for use in a wireless communication system, comprising:

an extract and split unit for receiving an input signal and splitting the input signal into even samples and odd samples;

two even midamble correlators for even sample processing, each even midamble correlator connected to said extract and split unit;

an even sample delay unit connected to one of said even midamble correlators;

an even correlator adder connected to the other of said even midamble correlators and said even sample delay unit;

an even sample accumulator connected to said even correlator adder;

two odd midamble correlators for odd sample processing, each odd midamble correlator connected to said extract and split unit;

an odd sample delay unit connected to one of said odd midamble correlators;

an odd correlator adder connected to the other of said odd midamble correlators and said odd sample delay unit;

an odd sample accumulator connected to said odd correlator adder; and

a frame tracker processor connected to said even sample accumulator and said odd sample accumulator.

7. The wireless transmit/receive unit according to claim 6, wherein said even sample delay unit and said odd sample delay unit each provide a 57 chip delay.

8. The wireless transmit/receive unit according to claim 6, wherein said frame tracker processor outputs

a first significant path location; and

a most significant path valid indicator.

9. The wireless transmit/receive unit according to claim 8, wherein said first significant path location and said most significant path valid indicator are used for frame synchronization.

10. An integrated circuit for use in a wireless communication system, comprising:

an extract and split unit for receiving an input signal and splitting the input signal into even samples and odd samples;

two even midamble correlators for even sample processing, each even midamble correlator connected to said extract and split unit;

an even sample delay unit connected to one of said even midamble correlators;

an even correlator adder connected to the other of said even midamble correlators and said even sample delay unit;

an even sample accumulator connected to said even correlator adder;

two odd midamble correlators for odd sample processing, each odd midamble correlator connected to said extract and split unit;

an odd sample delay unit connected to one of said odd midamble correlators;

an odd correlator adder connected to the other of said odd midamble correlators and said odd sample delay unit;

an odd sample accumulator connected to said odd correlator adder; and

a frame tracker processor connected to said even sample accumulator and said odd sample accumulator.

11. The integrated circuit according to claim 10, wherein said even sample delay unit and said odd sample delay unit each provide a 57 chip delay.

12. The integrated circuit according to claim 10, wherein said frame tracker processor outputs

a first significant path location; and

a most significant path valid indicator.

13. The integrated circuit according to claim 12, wherein said first significant path location and said most significant path valid indicator are used for frame synchronization.